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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/161,512
Priority Filing Date ..... September 28, 1998
Inventor ..... James E. O'Toole et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2635
Priority Examiner ..... E. Holloway III
Attorney's Docket No. MI40-325
Title: Radio Frequency Data Communications Device

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

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AMENDMENTS

This is a preliminary amendment accompanying a Request for Continuation Application for the above-titled patent application. Prior to examining the application, please make the following amendments.

In the Specification

(i) On page 1, replace the paragraph beginning at line 4 and ending at line 6 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment, in accordance the provisions of 37 CFR §1.121(b)(1)(i)-(iii).

This application is a continuation of U.S. Patent Application Serial No. 09/161,512, filed on September 28, 1998, which is a divisional of U.S. Application Serial No. 08/705,043, filed on August 29, 1996, now U.S. Patent No. 6,130.602 (incorporated herein by reference), which claims priority from U.S. Provisional Application 60/017,900, filed May 13, 1996, titled "Radio Frequency Data Communication Device.

(ii) Replace the paragraph beginning at page 58, line 17 and ending at page 59, line 7 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment.

Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; (b) determining if the radio frequency signal is modulated and has a predetermined number of transitions per a predetermined period of time and, if so, proceeding to step (c); and, if not, returning to the sleep mode; and (c) determining if the modulated radio frequency signal has a predetermined number of transitions per a predetermined period of time different from the predetermined time of step (b)

and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

(iii) Replace the paragraph beginning at page 86, line 13 and ending at page 87, line 9 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment.

If the power source 18 is a battery, the battery can take any suitable form. Preferably, the battery type will be selected depending on weight, size, and life requirements for a particular application. In one embodiment, the battery 18 is a thin profile button-type cell forming a small, thin energy cell more commonly utilized in watches and small electronic devices requiring a thin profile. A conventional button-type cell has a pair of electrodes, an anode formed by one face and a cathode formed by an opposite face. Exemplary button-type cells are disclosed in several pending U.S. patent applications including U.S. Patent Application Serial No. 08/205,957, "Button-Type Battery Having Bendable Construction and Angled Button-Type Battery," listing Mark E. Tuttle and Peter M. Blonsky as inventors, now U.S. Patent No. 5,432,027; U.S. Patent Application Serial No. 08/321,251, "Button-Type Batteries and Method of Forming Button-Type Batteries," listing Mark E. Tuttle as inventor, now U.S. Patent No. 5,494,495; and U.S. Patent Application Serial No. 08/348,543, "Method of Forming Button-Type Batteries and a Button-Type Battery Insulating and Sealing Gasket," listing Mark E. Tuttle as inventor, now U.S. Patent No. 5,662,718. These patent applications

and resulting patents are hereby incorporated by reference. In an alternative embodiment, the battery 18 comprises a series connected pair of button type cells. Instead of using a battery, any suitable power source can be employed.

(iv) Replace the paragraph beginning at page 89, line 1 and ending at page 89, line 18 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment.

Various U.S. patent applications, which are incorporated herein by reference, disclose features that are employed in various alternative embodiments of the invention: 08/092,147, filed July 15, 1993, "Wake Up Device for a Communications System", now abandoned, and continuation application 08/424,827, filed April 19, 1995, "Wake Up Device for a Communications System", now U.S. Patent No. 5,790,946; 08/281,384, filed July 27, 1994, "Communication System Having Transmitter Frequency Control", now U.S. Patent No. 5,568,512; 07/990,918, filed December 15, 1992, now U.S. Patent No. 5,365,551, "Data Communication Transceiver Using Identification Protocol"; 07/899,777, filed June 17, 1992, "Radio Frequency Identification Device (RFID) and Method of Manufacture, Including an Electrical Operating System and Method," now abandoned; 07/921,037, filed July 24, 1992, "Anti-Theft Method for Detecting The Unauthorized Opening of Containers and Baggage," now abandoned; 07/928,899, filed August 12, 1992, "Electrically Powered Postage Stamp or Mailing or Shipping Label Operative with Radio Frequency (RF) Communications," now

abandoned; and 08/032,384, filed on March 17, 1993, "Modulated Spread Spectrum in RF Identification Systems Method," now U.S. Patent No. 5,539,775.

(v) Replace the paragraph beginning at page 137, line 17 and ending at page 137, line 24 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment.

Preferably, the above technique for mounting integrated circuit 16 to card 20 (of Fig. 4) consists of a flip-chip mounting technique. One example of a flip-chip mounting technique is disclosed in pending U.S. Patent Application Serial No. 08/166,747, "Process of Manufacturing an Electrical Bonding Interconnect Having a Metal Bond Pad Portion and Having a Conductive Epoxy Portion Comprising an Oxide Reducing Agent," listing Rick Lake and Mark E. Tuttle as inventors, now U.S. Patent No. 5,480,834 and incorporated herein by reference.

(vi) Replace the paragraph beginning at page 209, line 13 and ending at page 209, line 18 with the paragraph shown below in clean form. Another version of this paragraph, marked to show the changes made, is attached in a separate page from this amendment.

The multiplier cell originally developed by Gilbert employed bipolar junction transistors. It is also known to employ MOS transistors to produce

a Gilbert multiplier cell. See, for example, Analog Integrated Circuits for Communication, Principles, Simulation and Design, Donald O. Pederson and Kartikeya Mayaram, Kluwer Academic Publishers, Third Printing, 1994, pp. 431-433.

In the Claims

Cancel claims 1-252 and add new claims 253-284 as follows.

253. CMOS transmitter carrier circuitry configured to receive a digital clock signal, the circuitry comprising:

a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple and control circuitry to maintain a desired frequency, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to the voltage controlled oscillator and receiving the multiplied frequency, the divider circuitry being configured to divide by the predetermined multiple, and the divider circuitry having an output coupled to the control circuitry.

254. CMOS transmitter carrier circuitry in accordance with claim 253, wherein:

the phase locked loop includes a loop filter coupled to the voltage controlled oscillator, and the control circuitry comprises:

a phase-frequency detector coupled to the divider circuitry output ; and

a charge pump, the phase-frequency detector and the charge pump being coupled to the voltage controlled oscillator and to the loop filter, wherein the loop filter is a passive loop filter.

255. CMOS transmitter carrier circuitry in accordance with claim 253, wherein the voltage controlled oscillator has a plurality of outputs that are configured to be angularly spaced apart with respect to phase.

256. CMOS transmitter carrier circuitry in accordance with claim 255, further comprising a frequency doubler that receives at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

257. CMOS transmitter carrier circuitry in accordance with claim 256, wherein the frequency doubler comprises first and second Gilbert cells coupled together, a frequency generator configured to apply a first sinusoidal wave to the first Gilbert cell, and a phase shifter coupled between the first and second Gilbert cells to apply to the second Gilbert cell a sinusoidal wave that is shifted from the first sinusoidal wave.

258. CMOS transmitter carrier circuitry in accordance with claim 253, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the control circuitry.

259. CMOS transmitter carrier circuitry in accordance with claim 258, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

260. A CMOS transmitter configured to receive a digital clock signal, the transmitter comprising:

a phase locked loop including a voltage controlled oscillator multiplying the frequency of the digital clock signal by a predetermined multiple, control circuitry coupled to the phase locked loop to maintain a desired frequency, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier;

divider circuitry having an input coupled to at least one of the outputs of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry; and

a modulator coupled to the phase locked loop to use the transmitter carrier.

261. A CMOS transmitter in accordance with claim 260, wherein the voltage controlled oscillator has outputs that are spaced apart, with respect to phase in 45 degree intervals.

262. A CMOS transmitter in accordance with claim 261, wherein the predetermined multiple is sixteen.

263. A CMOS transmitter in accordance with claim 260, wherein the control circuitry comprises:

a passive loop filter;

a phase-frequency detector, the divider circuitry output being coupled to the phase-frequency detector; and

a charge pump coupled to the voltage controlled oscillator and to the loop filter.

264. A CMOS transmitter in accordance with claim 263, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

265. A CMOS transmitter in accordance with claim 264, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

266. An integrated circuit including carrier circuitry configured to provide a carrier for wireless communications, the carrier circuitry being configured to receive a digital clock signal, the carrier circuitry being defined by CMOS circuit elements, the carrier circuitry comprising:

a phase locked loop including a voltage controlled oscillator multiplying the frequency of the digital clock signal by a predetermined multiple, control circuitry configured compare the frequency and phase of the digital clock signal to a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and configured to maintain a desired frequency in response to the pump up and pump down signals, the charge pump being configured to receive the pump up and pump down signals and produce an output having a voltage that varies in response to the pump up and pump down signals, the voltage controlled oscillator having an output, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to the output of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry.

267. An integrated circuit in accordance with claim 266, wherein the divider circuitry output defines the second signal and the control circuitry comprises a loop filter, a phase-frequency detector receiving the digital clock signal and the second signal and performing the comparison, the frequency of the output of the voltage controlled oscillator being configured to vary depending on a voltage provided by the loop filter to the voltage controlled oscillator.

268. An integrated circuit in accordance with claim 267 wherein the loop filter is configured to filter the output of the charge pump.

269. An integrated circuit in accordance with claim 266 wherein the predetermined multiple is sixteen.

270. An integrated circuit in accordance with claim 266, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

271. An integrated circuit in accordance with claim 270, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

272. An integrated circuit including carrier circuitry configured to provide a carrier signal for wireless communications, the carrier circuitry being configured to receive a digital clock signal, the carrier circuitry being defined by CMOS circuit elements and comprising:

a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry configured to receive the digital clock signal and compare the frequency and phase of the digital clock signal with a second signal and configured to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and to the voltage controlled oscillator to maintain a desired frequency in response to the pump up and pump down signals, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to at least one of the outputs of the voltage controlled oscillator, the divider circuitry dividing by the predetermined multiple and having an output defining the second signal coupled to the control circuitry.

273. An integrated circuit in accordance with claim 272 wherein the predetermined multiple is sixteen.

274. An integrated circuit in accordance with claim 272 wherein the control circuitry comprises:

a passive loop filter coupled to the phase locked loop; and

a phase-frequency detector coupled to the charge pump;

and further comprising a first frequency doubler configured to receive at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

275. An integrated circuit in accordance with claim 274 and further comprising a second frequency doubler coupled to the first frequency doubler and that is configured to produce a signal with a frequency that is double the frequency of the signal produced by the first frequency doubler.

276. An integrated circuit in accordance with claim 272 and further comprising a first frequency doubler stage including a first frequency doubler configured to receive at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator, and a second frequency doubler that receives other of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

277. An integrated circuit in accordance with claim 276 and further comprising a second frequency doubler stage coupled to the first frequency doubler stage and that is configured to produce a signal with a frequency that is double the frequency of the signals produced by the first frequency doubler stage.

278. An integrated circuit in accordance with claim 272, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

279. An integrated circuit in accordance with claim 278, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

280. A communications system including a transmitter integrated circuit for wireless communications, the transmitter integrated circuit being configured to receive a digital clock signal, the transmitter integrated circuit being defined by CMOS circuit elements and comprising:

a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry configured to receive the digital clock signal and to compare the frequency and phase of the digital clock signal with a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and the voltage controlled oscillator to maintain a desired frequency in response to the pump up and pump down signals, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier;

divider circuitry having an input coupled to at least at least one of the outputs of the voltage controlled oscillator, the divider circuitry dividing by the predetermined multiple and having an output defining the second signal coupled to the control circuitry; and

a modulator coupled to the voltage controlled oscillator.

281. A communications system in accordance with claim 280, wherein the voltage controlled oscillator includes a plurality of stages, one of the stages including a first transistor having a control electrode defining a first input, and first and second power electrodes, wherein the first power electrode defines a first node, wherein the stage further includes a second transistor having a control electrode defining a second input, and having first and second power electrodes, wherein the first power electrode of the second transistor defines a second node, wherein the stage further includes a current source connected to the second power electrodes of the first and second transistors, the current source being configured to direct current away from the second power electrodes of the first and second transistors, and wherein the stage further includes a variable resistance configured to couple the first and second nodes to a supply voltage.

282. A communications system in accordance with claim 280, wherein the control circuitry comprises:

a passive loop filter coupled to the phase locked loop and to the charge pump; and

a phase-frequency detector coupled to the second signal and to the charge pump.

283. A communications system in accordance with claim 280, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

284. A communications system in accordance with claim 283, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

REMARKS

Claims 1-252 have been canceled and new claims 253-284 have been added.

The amendments to the specification update the status of related applications and corrects minor informalities noted during review. No new matter is added by the amendments to the specification.

Another version of these paragraphs, marked to show the changes made and employing underlining to show additions and brackets to identify deletions, and including numbered paragraphs (i)-(vi) to illustrate correspondence with the clean versions of these paragraphs, is attached on separate pages from this amendment, in accordance the provisions of 37 CFR §1.121(b)(1)(i)-(iii).

New claims 253-284 are supported by text appearing at p. 83, line 5 through p. 279, line 3 of the specification as originally filed.

New claims 253-284 are also supported by p. 193, line 9 et seq. and associated Figs. of the specification as originally filed.

New claims 253-284 are also supported by p. 175, line 8 through p. 217, line 24, and in Figs. 8.0504, 8.050401, 8.050401AA-CK, 8.050402, 8.050402AA-CJ, 8.050403, 8.050403AA-BI, 8.050405 and 8.050405AA-EJ of the specification as originally filed.

No new matter is added by new claims 253-284. New claims 253-284 distinguish over the art of record and are allowable.

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice

of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made.**"

Respectfully submitted,

Dated: May 30, 2004 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS

(i) This application is a continuation of U.S. Patent Application Serial No. 09/161,512, filed on September 28, 1998, which is a divisional of U.S. Application Serial No. 08/705,043, filed on August 29, 1996, now U.S. Patent No. 6,130,602 (incorporated herein by reference), which claims priority from U.S. Provisional Application 60/017,900, filed May 13, 1996, titled "Radio Frequency Data Communication Device."

(ii) Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; (b) determining if the radio frequency signal is modulated and has a predetermined number of transitions per a predetermined period of time and, if so, proceeding to step (c); and, if not, returning to the sleep mode; and [©] (c) determining if the modulated radio frequency signal has a predetermined number of transitions per a predetermined period of time different from the predetermined time of step (b) and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

(iii) If the power source 18 is a battery, the battery can take any suitable form. Preferably, the battery type will be selected depending on weight, size, and life requirements for a particular application. In one embodiment, the battery 18 is a thin profile button-type cell forming a small, thin energy cell more commonly utilized in watches and small electronic devices requiring a thin profile. A conventional button-type cell has a pair of electrodes, an anode formed by one face and a cathode formed by an opposite face. Exemplary button-type cells are disclosed in several pending U.S. patent applications including U.S. Patent Application Serial No. 08/205,957, "Button-Type Battery Having Bendable Construction and Angled Button-Type Battery," listing Mark E. Tuttle and Peter M. Blonsky as inventors, now U.S. Patent No. 5,432,027; U.S. Patent Application Serial No. 08/321,251, "Button-Type Batteries and Method of Forming Button-Type Batteries," listing Mark E. Tuttle as inventor, now U.S. Patent No. 5,494,495; and U.S. Patent Application Serial No. 08/348,543, "Method of Forming Button-Type Batteries and a Button-Type Battery Insulating and Sealing Gasket," listing Mark E. Tuttle as inventor, now U.S. Patent No. 5,662,718. These patent applications and resulting patents are hereby incorporated by reference. In an alternative embodiment, the battery 18 comprises a series connected pair of button type cells. Instead of using a battery, any suitable power source can be employed.

(iv) Various U.S. patent applications, which are incorporated herein by reference, disclose features that are employed in various alternative embodiments of the invention: 08/092,147, filed July 15, 1993, "Wake Up Device for a Communications System", now abandoned, and continuation application 08/424,827, filed April 19, 1995, "Wake Up Device for a Communications System", now U.S. Patent No. 5,790,946; 08/281,384, filed July 27, 1994, "Communication System Having Transmitter Frequency Control", now U.S. Patent No. 5,568,512; 07/990,918, filed December 15, 1992, now U.S. Patent No. 5,365,551, "Data Communication Transceiver Using Identification Protocol"; 07/899,777, filed June 17, 1992, "Radio Frequency Identification Device (RFID) and Method of Manufacture, Including an Electrical Operating System and Method," now abandoned; 07/921,037, filed July 24, 1992, "Anti-Theft Method for Detecting The Unauthorized Opening of Containers and Baggage," now abandoned; 07/928,899, filed August 12, 1992, "Electrically Powered Postage Stamp or Mailing or Shipping Label Operative with Radio Frequency (RF) Communications," now abandoned; and 08/032,384, filed on March 17, 1993, "Modulated Spread Spectrum in RF Identification Systems Method," [now allowed] now U.S. Patent No. 5,539,775.

(v) Preferably, the above technique for mounting integrated circuit 16 to card 20 (of Fig. 4) consists of a flip-chip mounting technique. One example of a flip-chip mounting technique is disclosed in pending U.S. Patent Application Serial No. 08/166,747, "Process of Manufacturing an Electrical

Bonding Interconnect Having a Metal Bond Pad Portion and Having a Conductive Epoxy Portion Comprising an Oxide Reducing Agent," listing Rick Lake and Mark E. Tuttle as inventors, now U.S. Patent No. 5,480,834 and incorporated herein by reference.

(vi) The multiplier cell originally developed by Gilbert employed bipolar junction transistors. It is also known to employ MOS transistors to produce a Gilbert multiplier cell. See, for example, *Analog Integrated Circuits for Communication, Principles, Simulation and Design*, Donald O. Pederson and Kartikeya Mayaram, [Kuwer] Kluwer Academic Publishers, Third Printing, 1994, pp. 431-433.